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IMPLEMENTATION OF AN ADVANCED MicroTCA.4-BASED DIGITIZER FOR MONITORING COMB-LIKE BEAM AT THE J-PARC LINAC

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Abstract

The Japan Proton Accelerator Research Complex (J-PARC) linac beam pulse, generated by a beam chopper system placed at the MEBT, comprises a series of intermediate pulses with a comb-like structure synchronized with the radio frequency of the rapid cycling synchrotron (RCS). The sequentially measuring and monitoring the comb-like beam pulse ensures the beam stability with less beam loss at the current operation and higher beam intensity scenarios at the J-PARC. However, signal processing as a function of the pulse structure is challenging using a general-purpose digitizer, and monitoring the entire macro pulse during the beam operation is unavailable. To this end, an advanced beam monitor digitizer complying with the MicroTCA.4 (Micro Telecommunications Computing Architecture.4) standard, including digital signal processing functions, has been developed. This paper reports the implementation, performance evaluation, and the first results of this unique beam monitor digitizer.

INTRODUCTION

The Japan Proton Accelerator Research Complex (J-PARC) linac front-end comprises a negative hydrogen H^- ion source (IS), low-energy beam transport line (LEBT), 3 MeV radiofrequency quadrupole linac (RFQ), medium-energy beam transport line (MEBT1), housing two buncher cavities and RF choppers, 50 MeV drift-tube linac (DTL), 190.8 MeV separated type DTL (SDTL), and 400 MeV annular ring coupled structure ACS [1], see Fig. 2. A 50 mA H^- beam is injected into the rapid cycling synchrotron (RCS) through an L3BT (linac-to-3-GeV RCS beam transport) line. The linac also has an additional line, called medium-energy beam transport line 2 (MEBT2), which is equipped with two buncher cavities (B1 and B2).

Figure 1 shows the time structure of the beam from the linac. The IS generates macro-pulses of widths ranging from 50 to 500 μs (ω_{ma_p}). The beam pulse is formed by an RF chopper system [2] placed at MEBT1 and consists of a series of intermediate pulses with a comb-like structure, synchronized with RF frequency (f_{rf}) of the RCS ring. The beam is modulated by an RCS chop signal from the RCS low-level RF (LLRF) system [3]. It has different patterns in chopped-beam operations to achieve the comb-like structure. Thus, relying on this signal, the linac provides various pulse structures with different intermediate pulse widths (ω_{int_p}), thinning rates (TRs), and 1-bunch operation for the Material and Life Science Experimental Facility (MLF) and main ring (MR) in J-PARC [4].

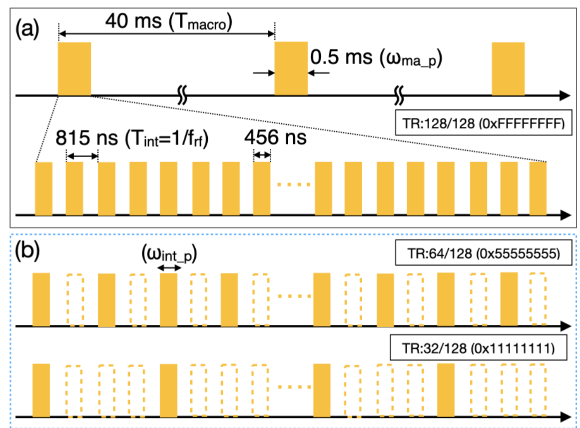

Figure 1: (a) Time structure of the linac beam; macro-pulses (upper), intermediate pulses (lower), (b) intermediate pulses with different thinning rates. 0xFFFFFFFF denotes the existence of all intermediate pulses in a macro-pulse, while dashed orange color blocks represent thinned-out pulses.

Numerous beam monitors are employed in J-PARC linac, such as the beam current monitor (slow current transformer, SCT), beam phase monitor (fast current transformer, FCT), and beam position monitor (BPM) [5, 6]. The extant WE7000 measurement station [7], has proven reliable over the past 15 years. However, obsolescence and the desire to monitor the entire macro-pulse necessitate the development of a new monitoring system. Monitoring the entire macro-pulse while performing signal processing in a field-programmable gate array (FPGA) during beam operation with a general-purpose digitizer is challenging. Consequently, we developed a new beam monitor digitizer (henceforth called "BMONDIG"), which complies with MicroTCA.4 (Micro Telecommunications Computing Architecture.4) standards and includes a digital signal processing (DSP) function. It sequentially measures the comb-like beam together with the duty cycle and averaging calculation processes, enabling the monitoring of the linac beam pulse structure. The aim is to achieve stable beam operation with lower beam loss for all intensities at J-PARC. This paper introduces the new monitor digitizer, its installation procedure, and the test results of beam pulse measurements.

HARDWARE

The BMONDIG architecture, as shown in Fig. 3, was implemented by the Mitsubishi Electric TOKKI Systems

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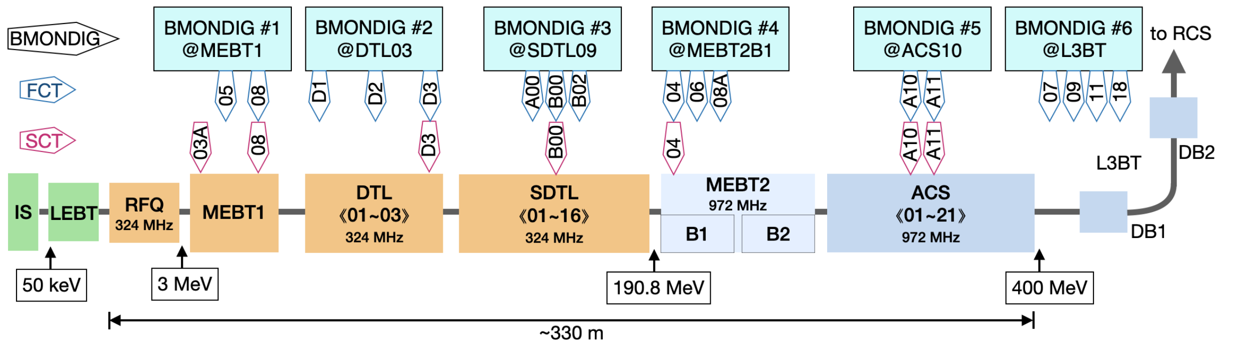

Figure 2: J-PARC linac configuration; turquoise color blocks represent new digitizers installed at corresponding stations.

Corporation (MELOS). The new MTCA.4-based digitizer was evaluated using an A/D•D/A signal processing board [8], consisting of an advanced mezzanine card (AMC) and a rear transition module (μRTM). The board includes eight analog-to-digital converters (ADCs) operating at 370 MSPS (max.) with 16 bits of resolution and 800 MHz bandwidth, and two digital-to-analog converters (DACs). The DC-coupled ADCs measure FCT and SCT signals, whereas 324 MHz RF signals from the BPMs are acquired using AC-coupled ADCs. The μRTM module has a small form factor pluggable (SFP) module for optical communication, a digital input/output (DIO), and an RJ-45 connector. The AMC and μRTM were connected through a ZD connector (Zone3).

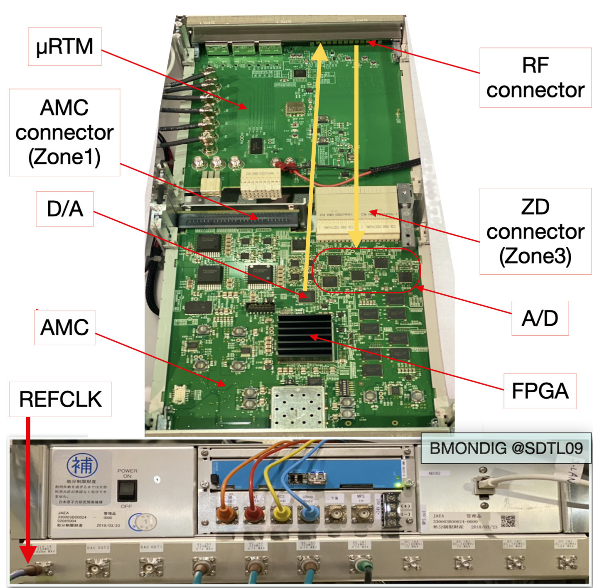

Figure 3: (Color online) Photograph of BMONDIG; (top) A/D•D/A board and μRTM, (bottom) front view of chassis.

FIRMWARE AND SOFTWARE

The firmware design was installed on a Zynq XC7Z045-1FFG900C FPGA on the A/D•D/A board. The firmware implements fast real-time functions for beam monitor signals, including raw data acquisition, duty, averaging of intermediate pulse amplitude, beam position and transmission calculations, and interlock protection, as illustrated in Fig. 4.

The design also enables point data and waveform monitoring of the beam pulses. A 144 MHz clock for each block is generated by an on-board phase-locked loop (PLL). The ADCs sample a comb-like beam when the beam gate is ON, that is, the beam starts. Once the RCS chop signal is realized on the digitizer, the average amplitude of each intermediate pulse is calculated. The processor runs the embedded Linux OS and integrates the experimental physics and industrial control system (EPICS) input/output controller (IOC) for data communication. A control system studio (CSS)-based ergonomic and straightforward graphical user interface (GUI) enables the operator to monitor beam signals and set calculation parameters.

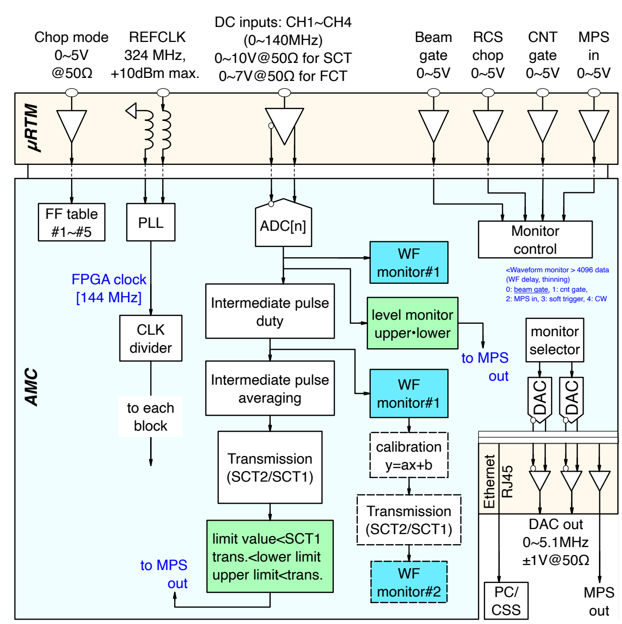

Figure 4: Simplified block diagram of firmware; signal processing scheme for only FCT and SCT signals is presented.

TEST RESULTS

Six new monitor digitizers were installed at MEBT1, DTL03, SDTL09, MEBT2B1, ACS10, and L3BT RF stations, as depicted in Fig. 2. After the installation, we measured the beam pulses from the FCT and SCT monitors using the new digitizers under different beam conditions.

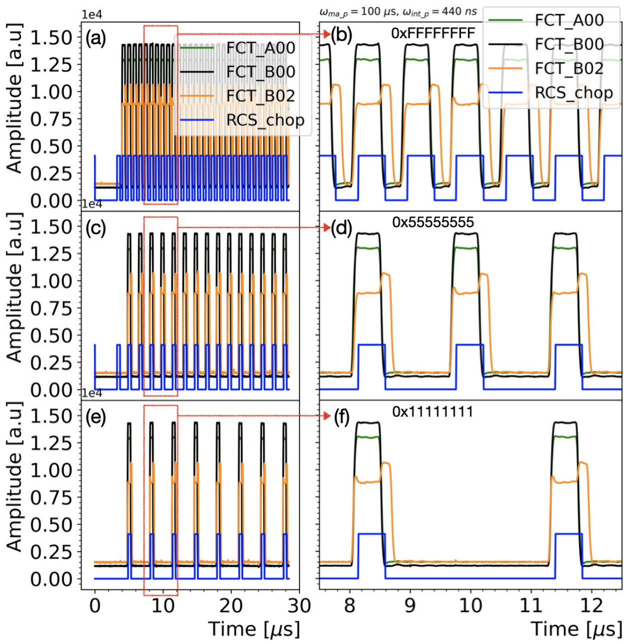

Figure 5: Intermediate pulses with different thinning rates (TRs); (a) and (b) pulses with TR of 0xFFFFFFFF, (c) and (d) pulses with TR of 0x55555555, (e) and (f) pulses with TR of 0x11111111. The graphics on the right column are the zoomed-in view of the left column graphics, respectively.

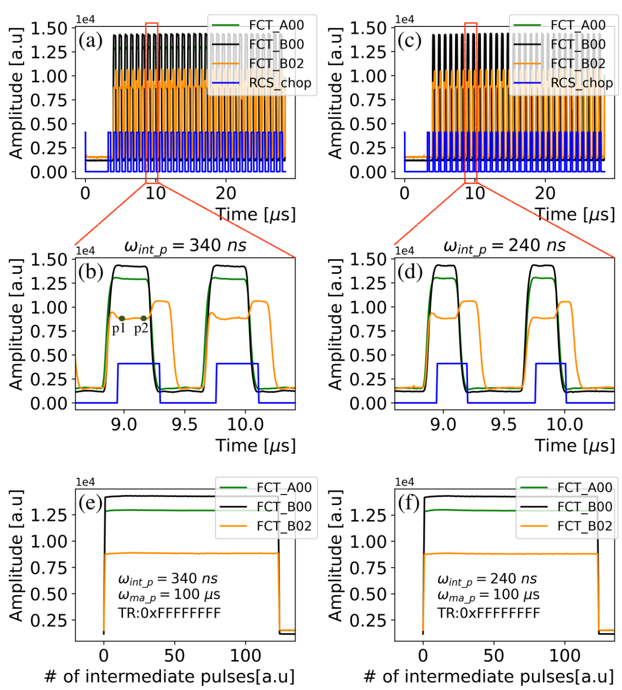

Figure 6: Intermediate pulses with different widths (ω_{int_p}); (a) and (b) pulses with a width of 340 ns, (c) and (d) pulses with a width of 240 ns, (e) and (f) average amplitude waveforms for intermediate pulses with widths of 340 ns and 240 ns, respectively.

The intermediate pulses, of width 440 ns, in a macro-pulse with different TRs are shown in Fig. 5. Figure 6 illustrates pulses with different widths at a thinning rate of 0xFFFFFFFF. The monitored values are averaged for each intermediate pulse within the range of the start and stop points (p1 and p2) by determining the timing of the RCS chop signal. Thus, a two-dimensional array corresponding to the intermediate pulse number can be displayed on the horizontal axis (Fig. 6(e) and (f)), and the vertical axis represents the average amplitude of all intermediate pulses. The ω_{ma_p} macro-pulse width was 100 μs for both studies, and data from the FCT monitors were acquired using the SDTL09 digitizer. Meanwhile, the intermediate pulses with a ω_{int_p} width of 440 ns from the SCT monitors were measured using several new digitizers, as shown in Fig. 7.

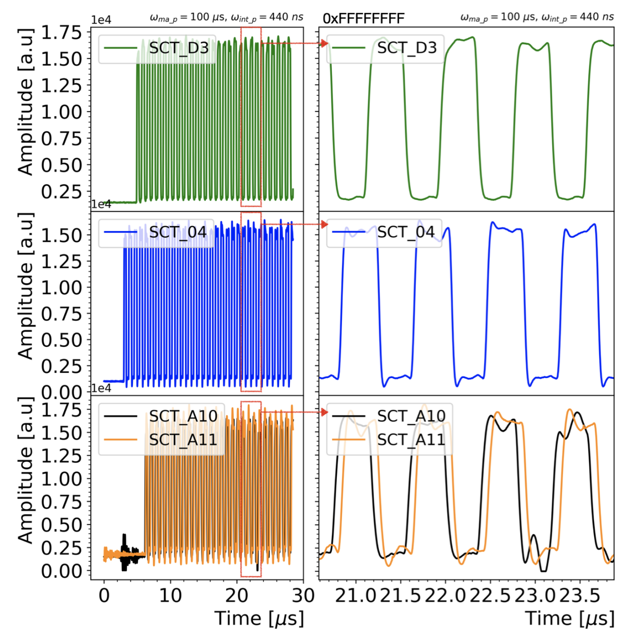

Figure 7: D3, 04, A10, and A11 SCT signals measured on the digitizers installed at DTL3, MEBT2B1 and ACS10, respectively (left column) and zoomed-in view of the intermediate pulses (right column).

CONCLUSIONS AND FUTURE WORK

A unique beam monitor digitizer complying with MicroTCA.4 standards was developed to measure and monitor linac comb-like beam structures. Six new digitizers were installed at six RF stations in the linac klystron gallery. The new digitizers successfully measured and monitored the linac beam pulses under different operating conditions. Meanwhile, BPM measurements, calculations, and FPGA design development are underway.

ACKNOWLEDGMENTS

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